In the Specification:

Please replace the paragraph beginning on page 4, line 31 with the following:

The correction algorithm discussed above with respect to block 14 in FIG. 1 is now described according to one embodiment of the invention. To reduce the algorithmic complexity, we assume that the standard deviations of the gate-delays are additive, i.e., we assume a perfect positive correlation between gate-delay variations along any path. If we assume that the path delay distributions remain Gaussian, then we can propagate the predetermined yield point (99% (i.e., $\mu+3\sigma$), for example) to the primary output. More specifically, we assume that

$$\mu_{1+2}+k\sigma_{1+2}=\mu+k\sigma=\mu_1+k\sigma_1+\mu_2+k\sigma_2 \quad (1)$$

where μ is the mean, σ is the standard deviation of the performance distribution of gates, and $\mu+k\sigma$ denotes a certain level of parametric yield. This also enables us to use STA instead of SSTA to verify the σ-slack correctness of the circuit.